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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/633,257	07/31/2003	William B. Boyle	K35A1307	4789

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EXAMINER	
KO, DANIEL BOKMIN	
ART UNIT	**PAPER NUMBER**
2189	

DATE MAILED: 03/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/633,257	BOYLE, WILLIAM B.	
	Examiner	Art Unit	
	Daniel B. Ko	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

This final office action is responsive to the amendment filed on 01/20/2006. Applicant amended claims 1, 17 and 18. Accordingly, claims 1-20 are pending.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

1. Claims 1-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Regarding claims 1, 17 and 18, a cache demand circuit adapted to: a) receive a memory address and a memory access signal. I assume that the memory address and the memory access signal are received from micro-controller request. In part b) micro-controller cache system to fetch data stored in the received memory address from the remote memory... prior to micro-controller request for the data stored in the received memory address. How can the invention fetch data stored in the received memory address before a micro-controller request for the data? Or how can invention receives the memory address and the memory access signal before the micro-controller make a request? Claims 2-16 and 19-20 are rejected based on dependency.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-3, 10-12, 14, and 17 are rejected under 35 U.S.C. 102(e) as being anticipated by Grimsrud et al. (US Patent 7,000,077 B2), hereinafter simply Grimsrud.

Regarding claims 1 and 17, Grimsrud teaches a disk drive control system comprising:

a micro-controller (Fig. 3, micro controller 40; column 2, lines 6-9);

a micro-controller cache system adapted to store micro-controller data for access by the micro-controller (Fig. 3, storage cache 50; column 2, lines 17-23);

a buffer manager adapted to provide the micro-controller cache system with micro-controller requested data stored in a remote memory (Fig. 3, storage buffer 46; column 2, lines 9-12); and

a cache demand circuit (Fig. 3, prefetch algorithms 112) adapted to:

a) receive a memory address and a memory access signal (column 6, lines 20-30), and

b) cause the micro-controller cache system to fetch data stored in the received memory address from the remote memory via the buffer manager based on the received memory address and memory access signal prior to a micro-controller request for the data stored in the received memory address (column 6, lines 20-38).

Regarding claim 2, Grimsrud teaches a disk drive control system, wherein the memory address and a memory access signal are received from the micro-controller and wherein the memory address is an address of data residing in the remote memory (column 6, lines 20-30).

Regarding claim 3, Grimsrud teaches a disk drive control system, wherein the memory access signal is a write signal received from the micro-controller (column 6, lines 20-38).

Regarding claim 10, Grimsrud teaches a disk drive control system, wherein the micro-controller cache system comprises a cache memory having a plurality of cache segments wherein the fetched data is stored in a cache segment of the memory (column 6, lines 11-30).

Regarding claim 11, Grimsrud teaches a disk drive control system, wherein the micro-controller cache system is adapted to receive the memory address and the memory access signal from the cache demand circuit (column 6, lines 20-30).

Regarding claim 12, Grimsrud teaches a disk drive control system, wherein the buffer manager is in communication with a plurality of control system clients and provides client-requested data to the clients from the remote memory (column 1, lines 46-62; column 2, lines 9-12).

Regarding claim 14, Grimsrud teaches a disk drive control system, wherein the remote memory comprises a dynamic random access memory (DRAM) (column 1, lines 23-29).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 4, 8, 13, 15, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Grimsrud et al. (US Patent 7,000,077 B2) in view of Hoskins (US Patent 6,789,132 B2).

Regarding claim 4, Grimsrud teaches a disk drive control system comprising:

a micro-controller (Fig. 3, micro controller 40; column 2, lines 6-9);

a micro-controller cache system adapted to store micro-controller data for access by the micro-controller (Fig. 3, storage cache 50; column 2, lines 17-23);

a buffer manager adapted to provide the micro-controller cache system with micro-controller requested data stored in a remote memory (Fig. 3, storage buffer 46; column 2, lines 9-12); and

a cache demand circuit (Fig. 3, prefetch algorithms 112) adapted to:

a) receive a memory address and a memory access signal (column 6, lines 20-30), and

b) cause the micro-controller cache system to fetch data stored in the received memory address from the remote memory via the buffer manager based on the received memory address and memory access signal prior to a micro-controller request for the data stored in the received memory address (column 6, lines 20-38).

Grimsrud fails to teach an the memory access signal is a priority interrupt signal. Hoskins teaches a data storage control module for controlling operational processes comprising preemptive, non-preemptive, and scheduler modules (See abstract). Hoskins teaches an interrupt circuit adapted to interrupt the micro-controller based on a transmitted interrupt signal (See, Fig. 2, element 230, host interrupt module; column 10, lines 56-67).

At the time of invention it would have been obvious to a person of ordinary skill in the art to combine the Grimsrud with Hoskins. The motivation for doing so would have been a proper handle of time critical operation. Hoskins states that the preemptive control modules handle time critical operation, such as responses to interrupts from a host computer (column 3, lines 5-7). Therefore, it would have been obvious to implement Grimsrud's pre-fetch with Hoskins' interrupt to minimize delays.

Regarding claim 8, Hoskins teaches a disk drive control system, wherein the memory access signal is a priority interrupt signal (Fig. 2, element 230, host interrupt module; column 10, lines 56-67). Hoskins teaches a preemptive multi-tasking which means there is a priority.

Regarding claim 13, Hoskins teaches a disk drive control system, wherein the plurality of control system clients comprises at least one of a disk subsystem, an error correction code subsystem, and a host interface subsystem (column 30, lines 59-66).

Regarding claim 15, Hoskins teaches a disk drive control system, wherein the memory access signal is a servo-interrupt signal (column 10, lines 56-67).

Regarding claim 16, Hoskins teaches a disk drive control system, wherein the memory access signal is a host-interrupt signal (Fig. 2, element 230, host interrupt module; column 10, lines 56-67).

4. Claims 5-7, 9 and 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Grimsrud et al. (US Patent 7,000,077 B2) and Hoskins (US Patent 6,789,132 B2), and further in view of Uchihori (US patent 6,516,389 B1).

Regarding claim 18, Grimsrud and Hoskins teach a disk drive control system comprising:

a micro-controller (See Grimsrud, Fig. 3, micro controller 40; column 2, lines 6-9);

a micro-controller cache system adapted to store micro-controller data for access by the micro-controller (See Grimsrud, Fig. 3, storage cache 50; column 2, lines 17-23);

a buffer manager adapted to provide the micro-controller cache system with micro-controller requested data stored in a remote memory (See Grimsrud, Fig. 3, storage buffer 46; column 2, lines 9-12);

a interrupt circuit adapted to interrupt the micro-controller based on a transmitted interrupt signal (See Hoskins, Fig. 2, element 230, host interrupt module; column 10, lines 56-67); and

a cache demand circuit (See Grimsrud, Fig. 3, prefetch algorithms 112) adapted to:

a) receive a memory address from the micro-controller (See Grimsrud, column 4, lines 4-7; column 6, lines 20-30) and the transmitted interrupt signal from the interrupt circuit (See Hoskins, Fig. 2, element 230, host interrupt module; column 10, lines 56-67), and

b) cause the micro-controller cache system to fetch data stored in the memory address from the remote memory via the buffer manager prior to a micro-controller request for the data stored in the memory address (column 4, lines 4-7; column 6, lines 20-38).

Grimsrud nor Hoskins fails to teach a request for the data stored in the predetermined memory address. Uchihori teaches an accessing predetermined memory address (column 2, lines 59-67; column 3, lines 1-9; column 8, lines 12-20; column 9, lines 1-17).

At the time of invention it would have been obvious to a person of ordinary skill in the art to combine the Grimsrud and Hoskins with Uchihori. The motivation for doing so would have been an increasing the disk cache hit rate, and speed up the data readout (See Uchihori, column 16, lines 25-28).

Regarding claims 5-7, and 9, Grimsrud and Uchihori teach a disk drive control system wherein the memory address is a predetermined memory address (See Uchihori, column 2, lines 59-67; column 3, lines 1-9; column 8, lines 12-20; column 9, lines 1-17) received prior to the memory access signal (See Grimsrud, column 4, lines 4-7).

Regarding claims 19-20, Grimsrud, Hoskins and Uchihori teach a disk drive control system wherein the memory address is a predetermined memory address (See Uchihori, column 2, lines 59-67; column 3, lines 1-9; column 8, lines 12-20; column 9, lines 1-17) received prior to the memory access signal (See Grimsrud, column 4, lines 4-7).

Response to Arguments

Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel B. Ko whose telephone number is 571-272-8194. The examiner can normally be reached on 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald G. Bragdon can be reached on 571-272-4204. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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